Datasheet
MM1200 – 6 Channel SPST Relay

Preliminary Product Overview

Description

The MM1200 device is a 6-channel SPST Micro Relay developed and manufactured by Menlo Micro. It is intended for power and signal switching applications in both DC and AC circuits.

Reliable and innovative, Menlo Micro's Ideal-Switch technology enables robust switches capable of 1.0 A per channel. The technology also enables low on-state contact resistance and high off-state isolation with greater than 3 billion switching cycles at elevated +85ºC temperatures. Each switch is normally open (NO) and individually controlled by a Serial Peripheral Interface (SPI) bus. An external +5 VDC logic supply and high voltage +75 V_{DC} bias source is required for operation of the internal switch driver.

Features

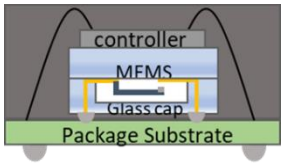
- 1.0 A per channel / 3.0 A Total Current
- Maximum Voltage (AC or DC): +150 V
- Low On-State Resistance < 1.0 Ω
- 10 GΩ Input to Output Isolation
- < 10us Switching Time
- High Reliability > 3 Billion Switching Operations
- Integrated SPI Bus Control
- 6mm x 6mm x 1.3mm BGA Package

Markets

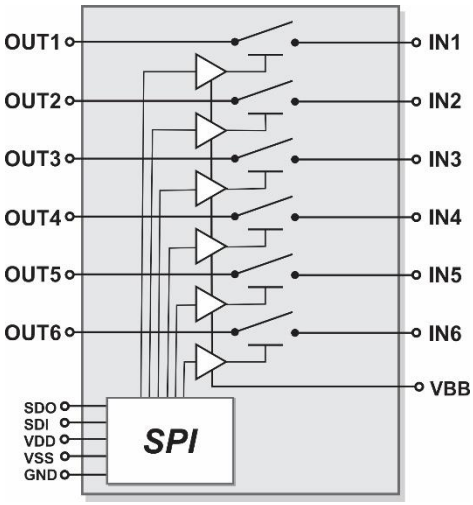
- Test & Measurement
- Wireless Charging
- Scientific and Medical
- Telecom

Applications

- High Density Switch Matrixes
- Automated Test and Measurement Systems
- Mechanical Relay Replacement



Functional Diagram



Available Options

Part Number	Package	Temperature Range
MM1200-00	6mm x 6mm 49 ball BGA	-40°C to +85°C
MM1200-00-E	6mm x 6mm 49 ball BGA	-40°C to +100°C

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM1200 should be restricted to the limits indicated in Table 2 recommended operating conditions listed below.

Electrostatic Discharge (ESD) Safeguards

When handling the MM1200, observe the same precautions as with any other ESD sensitive devices. Precautions must be taken to avoid exceeding the ratings specified in Table 1 below.

Susceptibility to Latch-Up

The MM1200 device is generally not susceptible to switch latch-up condition, however the following power-up and power-down sequences re recommended:

- Power-Up: Apply VDD, set all inputs to known state, apply VBB
- Power-Down: Remove VBB, Remove VDD

The high voltage supply (VBB) may be applied and removed as required when VDD is present.

Table 1 Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Logic Supply Voltage (VDD)		7.5	V_{DC}
High Voltage Bias Supply (VBB)		90	V_{DC}
Serial Input Voltage, Low / High	-0.3	VDD + 0.3	V
DC Voltage Rating / Switch		+/- 150	V

[1] All parameters must be within recommended operating conditions. Maximum DC and AC power can only be applied during the on-state condition (cold-switched condition).

DC Current Rating / Switch		1000	mA
Operating Temperature Range	-40	+85 (MM1200-00) +100 (MM1200-00-E)	˚C
ESD Voltage All Pins[2]		250	V
Storage Temperature Range	-70	+150	ºC

Electrical Characteristics

Table 2 Recommended Operating Conditions, DC and AC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
AC Signal Frequency Range	0		1000	MHz
AC/DC Current / Channel			1000	mA
Total Current per Device			3000	mA
Peak Current / Channel @ 10% DC[3]			7000	mA
On-State Resistance / R_{ON}		500	1000	mΩ
Off State Input to Output Isolation / R_{OFF}	TBD	10		GΩ
Channel to Channel Isolation	TBD	10		GΩ
Off / Open State Switch Rated Voltage (Input to Output)[4]	-150		+ 150	V_{DC}
Off / Open State Switch Rated Voltage (Output to VSS)	-45		45	V_{DC}

[2] HBM or CDM
[3] Duty Cycle based on 10 us period. Average current over period and all channels must NOT exceed *Total Current per Device* specification.
[4] The voltage difference between RF Output (Beam) pin and Supply Voltage Return (VSS) pin must be ±2.5V.

On / Closed State Switch Rated Voltage (Output to VSS)	-45		45	V_{DC}
Switching Time		8	10	µsec
Full Cycle Frequency			10	kHz
Mechanical Reliability	$3x10^9$			Cycles
Electrical Reliability (1.0V, 10mA)	$3x10^9$			Cycles
Leakage Current @ 150 Volts		< 19		pA

Table 2 Recommended Operating Conditions, DC and AC Electrical Characteristics (continued)

Parameter	Minimum	Typical	Maximum	Unit
High Voltage Gate Bias (VBB)	72.5	75	77.5	V_{DC}
High Voltage Gate Bias (VBB) Supply Current			0.1	mA
Low Voltage Supply (VDD)	4.5	5.0	5.5	V_{DC}
Low Voltage Supply (VDD) Current (standby)			50	uA
SPI Clock Frequency (CLK)	0.5		5	MHz
SPI Logic Level (High)	3.5	5.0	5.3	V
SPI Logic Level (Low)	-0.3	0.0	0.8	V
SPI Pulse Duration, clock high	100			nS
SPI Pulse Duration, latch enable high	100			nS
SPI Setup Time, data before clock	50			nS

SPI Hold Time, data after clock	50			nS
SPI Delay Time, clock to latch enable high	50			nS
SPI Propagation Delay Time, latch enable to output		300		nS
Operating Temperature Range	-40		+85 (MM1200-00) +100 (MM1200-00-E)	ºC

Typical Performance Characteristics

Note: *All measurements performed on MM1200-EVK test and evaluation board*

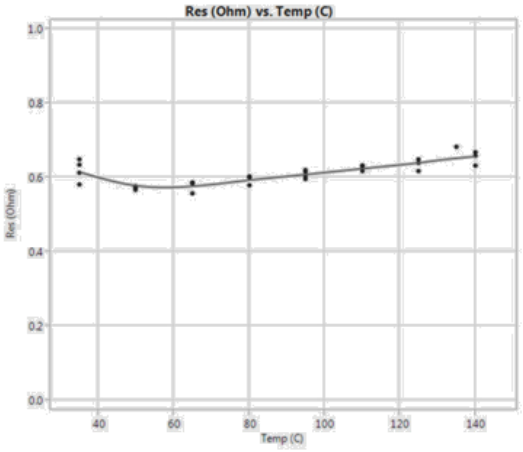


Figure 1 *Resistance vs Temperature*

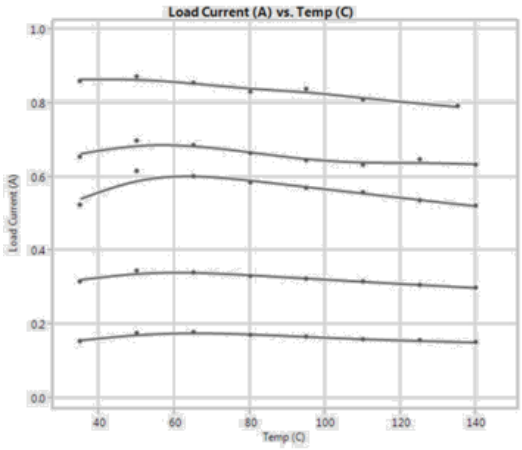


Figure 2 *Load Current vs Temperature*

49-Lead BGA Package Pin Out

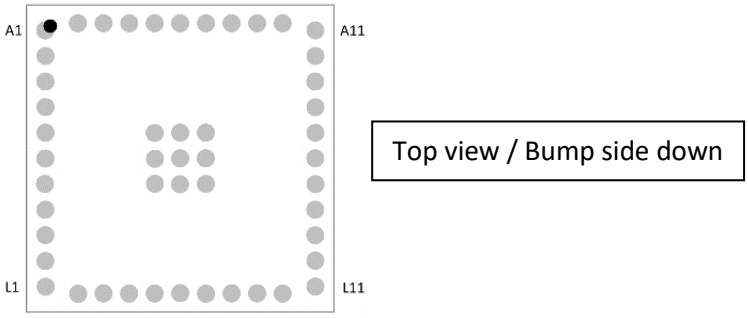


Table 3 Detailed Pin Description

Pin #	Function	Description	Pin #	Function	Description
A1, C1, J1, L1, L2, L4, L6, L8, L10, L11, J11, C11, A10, A11, A6, A8, A2, A4, E5, E6, E7, F5, F6, F7, G5, G6, G7	GND	Ground Reference	**L9**	IN5	Input (Contact 5)
B1	OUT1	Output (Beam 1)	**K11**	IN6	Input (Contact 6)
D1	BLNK	All Channels Off	**H11**	CLK	SPI Clock Input
E1	SDI	SPI Serial Data Input	**G11**	VSS	Supply Voltage Return
F1, D11	N/C	Do Not Connect	**F11**	VDD	+5 VDC Logic Supply
G1	VBB	High Voltage Supply	**E11**	LE	SPI Strobe Input
H1	SDO	SPI Serial Data Output	**B11**	OUT6	Output (Beam 6)
K1	IN1	Input (Contact 1)	**A9**	OUT5	Output (Beam 5)
L3	IN2	Input (Contact 2)	**A7**	OUT4	Output (Beam 4)

L5	IN3	Input (Contact 3)	**A5**	OUT3	Output (Beam 3)
L7	IN4	Input (Contact 4)	**A3**	OUT2	Output (Beam 2)

SPI Interface Gate Drive Control

Operating Description

The SPI bus gate driver block and high voltage driver diagram is shown in Figure 3. The driver contains a 10-bit shift register, a 10-bit latch and 10 high voltage drivers. The MM1200 uses six bits for switch control. A logic “1” closes a switch. Registers 7,8,9 and 10 are not used. There is no reset function. To clear register content, new data must be clocked in.

The high voltage driver is controlled by the Clock, Data In, Latch Enable, and Blanking lines as follows:

- A 6-bit data word is serially loaded into the shift register on the positive edge of the clock. First bit loaded controls IN6/OUT6, last bit in controls IN1/OUT1.
- Parallel data is transferred to the output buffers through a 10-bit D latch while the latch enable input is pulsed high. Note: Only latches 1-6 are used.
- Data is latched (to the switches) when the Latch Enable is low.
- If Latch Enable remains high, the latches operate in transparent mode.
- When the Blanking is high; outputs are forced low.
- All inputs are compatible with 5.0 V CMOS levels or any other 5.0 V logic level outputs such as microcontroller GPIO outputs.
- Serial Data Out (SDO) may be used to cascade multiple devices by connecting SDO of the first device toe SDI of the next device. Other control signals should be shared between all the devices. In this case it is recommended to load 10-bit words consisting of 4 dummy bits and 6 switch control bits so that each word controls one switch.

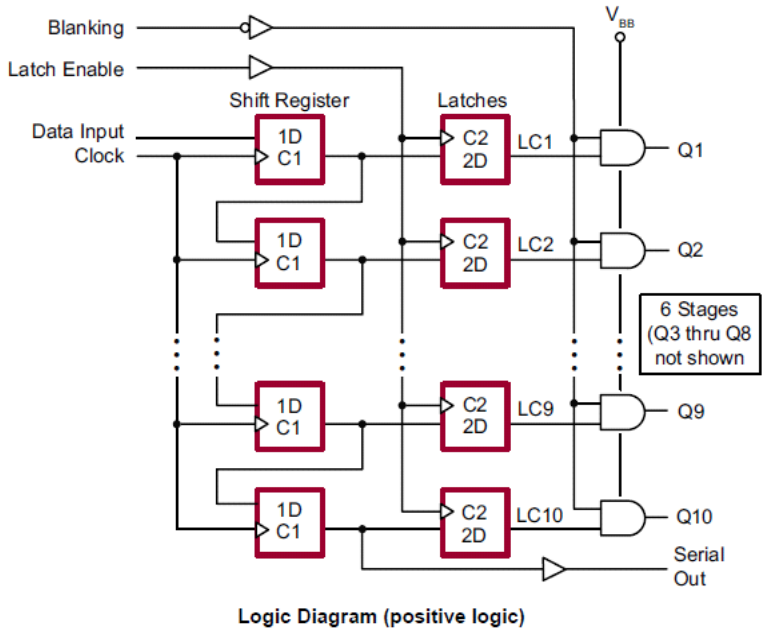


Figure 3 *High Voltage Gate Driver Block Diagram*

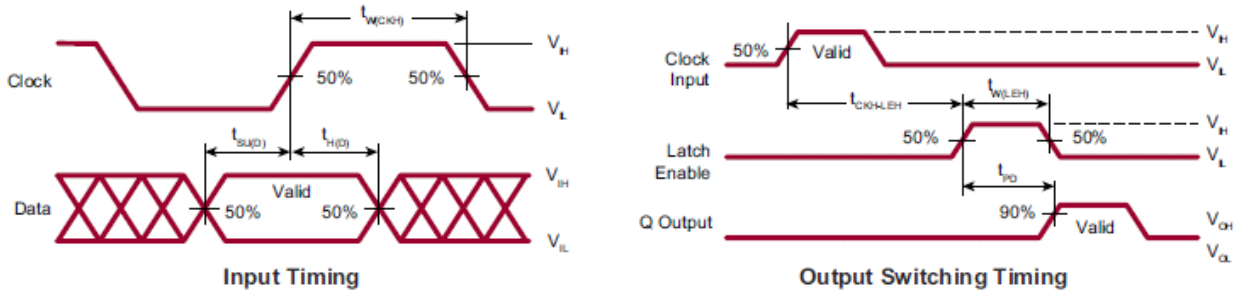


Figure 4 *Switching Waveforms*

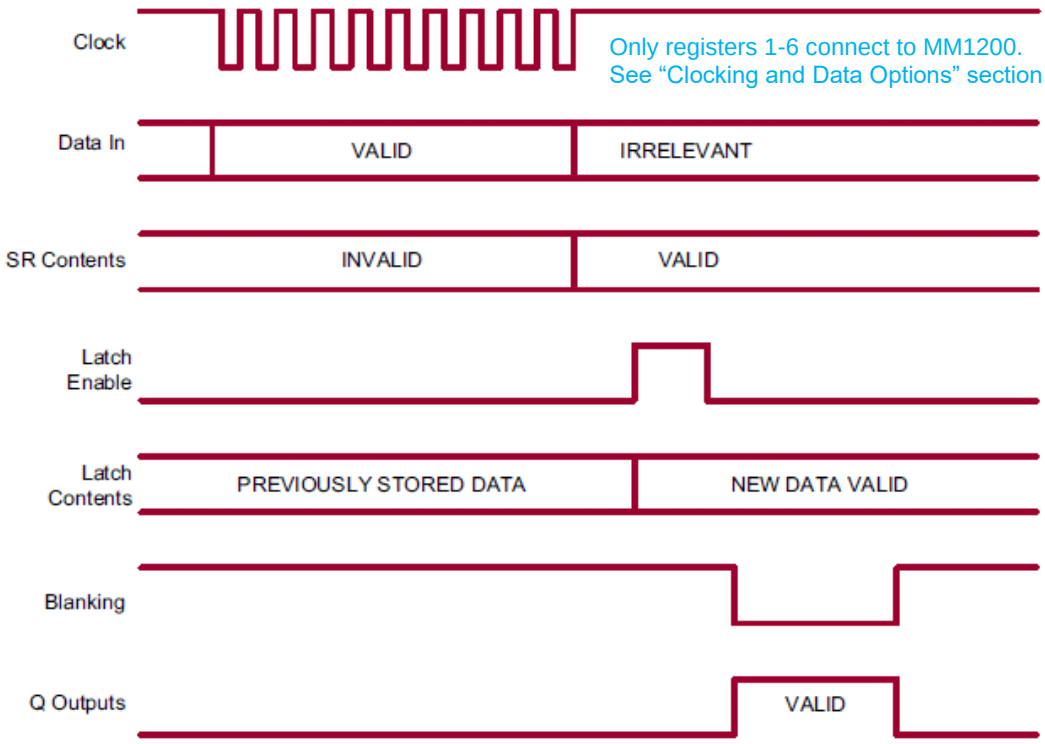


Figure 5 *Timing Diagram*

Table 4 Digital Control Functions

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \cdots\ I_{N-1}\ I_N$	Serial Data Output	LE Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \cdots\ I_{N-1}\ I_N$	Blanking Input	Output Contents $I_1\ I_2\ I_3\ \cdots\ I_{N-1}\ I_N$
H	↑	$H\ R_1\ R_2 \cdots R_{N-2}\ R_{N-1}$	R_{N-1}	---	---	---	---
L	↑	$L\ R_1\ R_2 \cdots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	↓	$R_1\ R_2\ R_3 \cdots R_{N-1}\ R_N$	R_N				
---	---	$X\ X\ X\ \cdots\ X\ X$	X	L	$R_1\ R_2\ R_3 \cdots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3 \cdots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3 \cdots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3 \cdots P_{N-1}\ P_N$
		---	---	---	$X\ X\ X\ \cdots\ X\ X$	H	$L\ L\ L\ \cdots\ L\ L$

Notes:
L = Low logic level, H = High logic level, X = Don't care, P = Present state, R = Previous state
↑ = Low to high transition
↓ = High to low transition

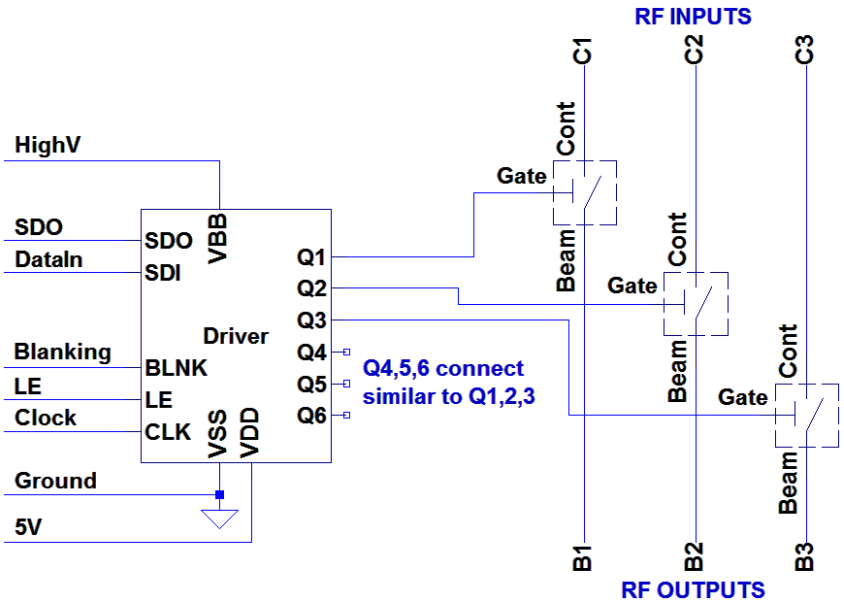


***Figure 6** Simplified Functional Block Diagram*

Clocking and Data Options

The driver section has a 10-bit shift register and latch. However, only registers 1-6 are connected to the 6 MM1200 channels in this device. Registers 7 to 10 are unused, except that data must be shifted through them if you wish to cascade devices. The MM1200 provides a Serial Data Output (SDO) pin, which enables cascading this device for additional switch channel applications. Other devices can be daisy-chained by connecting the SDO of one device to SDI of another.

Recommended PCB Layout and SMT Parameters

- PCB lands should be as shown in the pad pattern diagram
- Connect RFG node (floating shield inside the package) to RF Signal Ground
- Open space around the package can have grounded thru holes
- ENIG (Electroless Nickel Immersion Gold) pad surface finish
- 100 micron (µm) thick solder mask
- Type 3 or higher solder paste with no clean flux
- Component placement force not to exceed 100 grams

Recommended PCB Pad Pattern

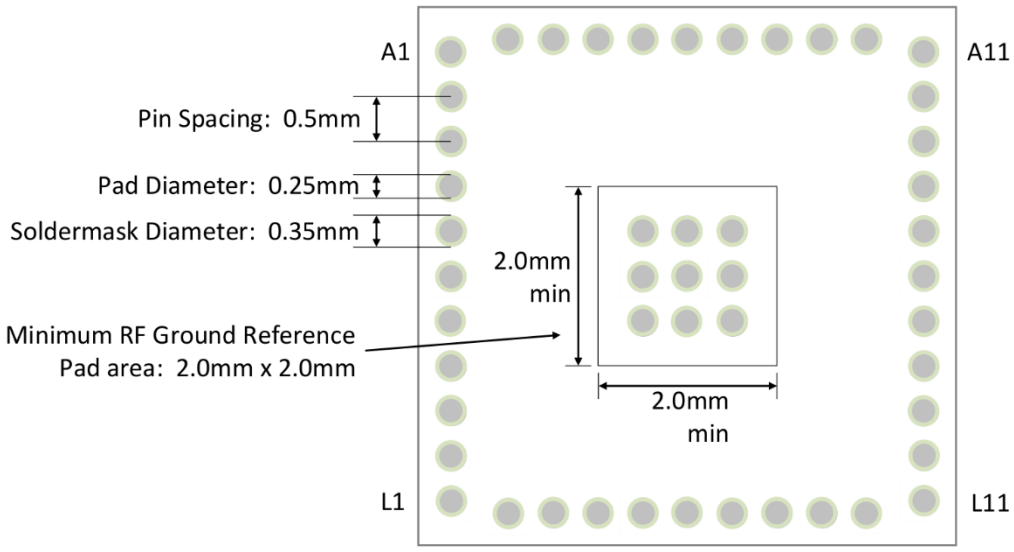
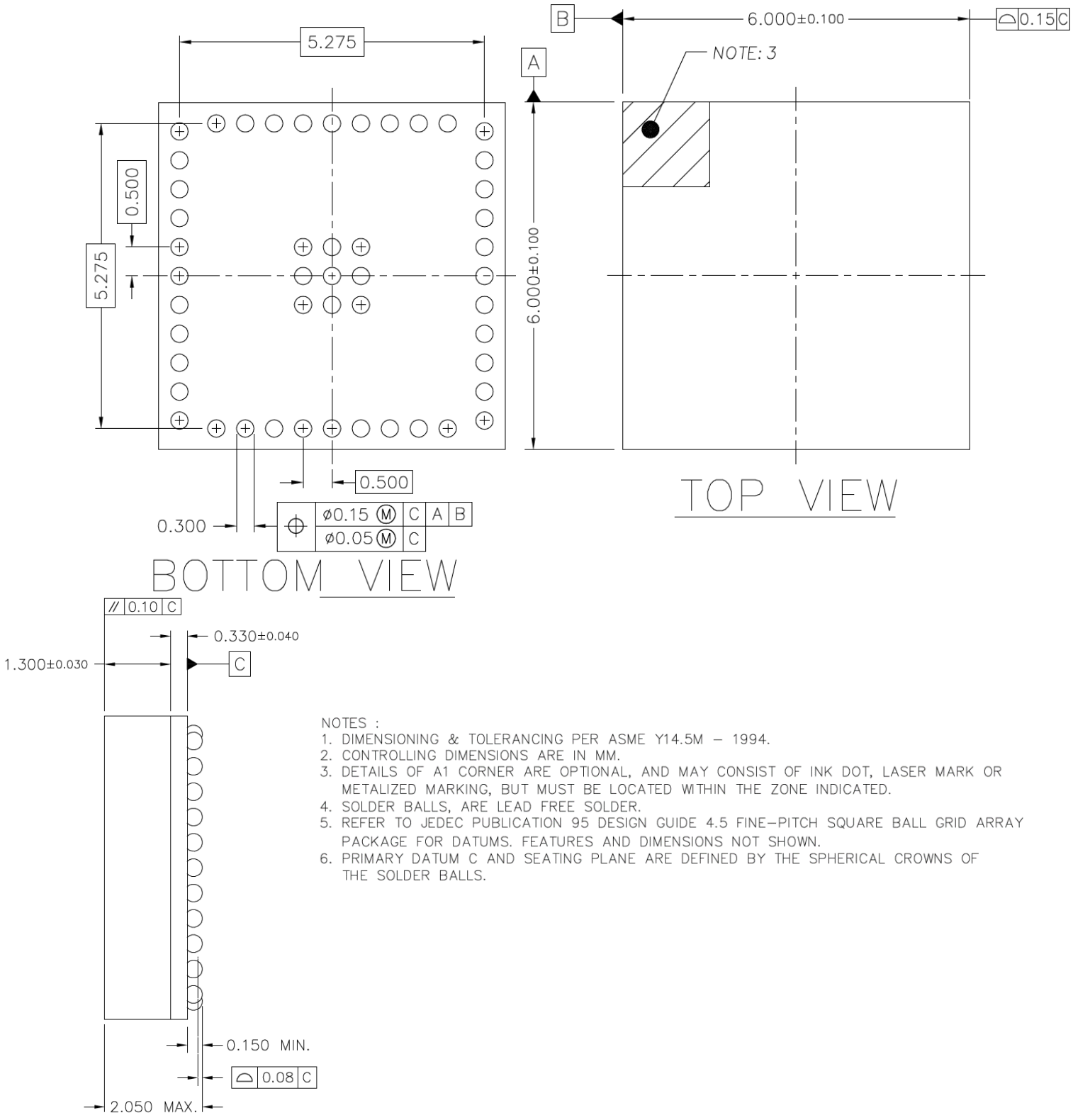


Figure 9 *Recommended PCB Pad Pattern*

Package Dimensions – 49 Lead Ball Grid Array

0.30mm Ball, 0.50mm Pitch

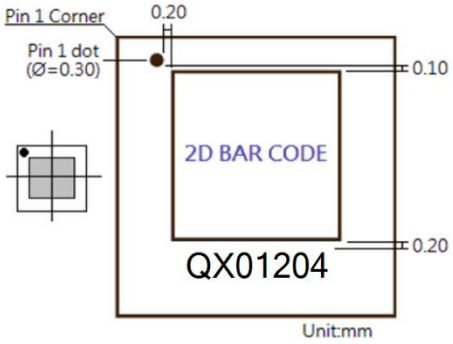


NOTES :

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSIONS ARE IN MM.
3. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
4. SOLDER BALLS, ARE LEAD FREE SOLDER.
5. REFER TO JEDEC PUBLICATION 95 DESIGN GUIDE 4.5 FINE–PITCH SQUARE BALL GRID ARRAY PACKAGE FOR DATUMS. FEATURES AND DIMENSIONS NOT SHOWN.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Package Marking Information

The MM1200 package marking and nomenclature is illustrated in Figure 10 below.



Dot ● = Pin 1 Indicator

Line 1 = 2D Bar Code

Line 2 = Device Part Number

Figure 10 *Package Markings*

Ordering Information

Part Number	Package	Packaging
MM1200-00	6mm x 6mm x 1.3mm BGA	Tape and Reel
MM1200-00-E	6mm x 6mm x 1.3mm BGA	Tape and Reel

Important Information

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Contact Information

Please contact Menlo Micro for the latest specifications, additional product information, test and evaluation boards, product samples, worldwide sales and distribution locations:

Internet: www.menlomicro.com

E-mail: sales@menlomicro.com

For product technical questions and application information: support@menlomicro.com