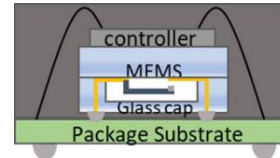


Preliminary Product Overview

Features

- 1.0 A per channel / 3.0 A Total Current
- Maximum Voltage (AC or DC): +150 V
- Low On-State Resistance < 1.0 Ω
- 10 G Ω Input to Output Isolation
- < 10us Switching Time
- High Reliability > 3 Billion Switching Operations
- Integrated SPI Bus Control
- 6mm x 6mm x 1.3mm BGA Package



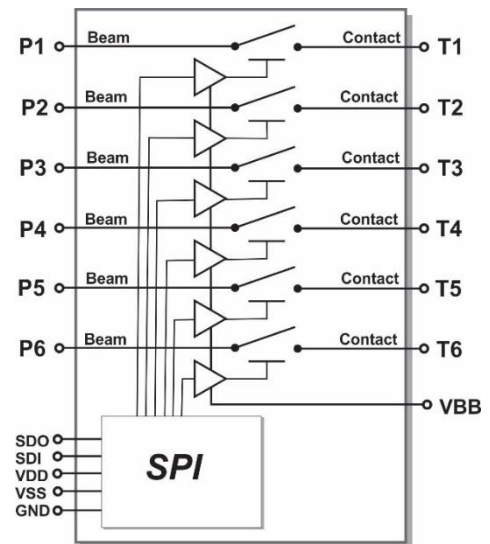
Markets

- Test & Measurement
- Wireless Charging
- Scientific and Medical
- Telecom

Applications

- High Density Switch Matrixes
- Automated Test and Measurement Systems
- Mechanical Relay Replacement

Functional Diagram



Description

The MM1200 device is a 6-channel SPST Micro Relay developed and manufactured by Menlo Micro. It is intended for power and signal switching applications in both DC and AC circuits.

Reliable and innovative DMS technology enables robust switches capable of 1.0 A per channel. The DMS technology enables low on-state contact resistance and high off-state isolation with greater than 3 billion switching cycles at elevated +85°C temperatures. Each switch is normally open (NO) and individually controlled by a Serial Peripheral Interface (SPI) bus. An external +5 VDC logic supply and high voltage +70 V_{DC} bias source is required for operation of the internal switch driver.

Available Options

Part Number	Package	Temperature Range
MM1200-00	6mm x 6mm 49 ball BGA	-40°C to +85°C
MM1200-00-E	6mm x 6mm 49 ball BGA	-40°C to +100°C

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM1200 should be restricted to the limits indicated in Table 2 recommended operating conditions listed below.

Electrostatic Discharge (ESD) Safeguards

When handling the MM1200, observe the same precautions as with any other ESD sensitive devices. Even though the MM1200 is protected from ESD damage, precautions must be taken to avoid exceeding the ratings specified in Table 1 below.

Susceptibility to Latch-Up

The MM1200 digital micro Relay is generally not susceptible to switch latch-up condition.

Table 1 Maximum Ratings¹

Parameter	Minimum	Maximum	Unit
Logic Supply Voltage (VDD)		7.5	V _{DC}
High Voltage Bias Supply (VBB)		90	V _{DC}
Serial Input Voltage, Low / High	-0.3	VDD + 0.3	V
DC Voltage Rating / Switch		+/- 150	V
DC Current Rating / Switch		1000	mA
Operating Temperature Range	-40	+85 (MM1200-00) +100 (MM1200-00-E)	°C
ESD Voltage All Pins ²		250	V
Storage Temperature Range	-70	+150	°C

¹ All parameters must be within recommended operating conditions. Maximum DC and AC power can only be applied during the on-state condition (cold-switched condition).

² Per Human-Body Model

Electrical Characteristics

Table 2 Recommended Operating Conditions, DC and AC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
AC Signal Frequency Range	0		1000	MHz
AC/DC Current / Channel			1000	mA
Total Current per Device			3000	mA
Peak Current / Channel @ 10% DC ³			7000	mA
On-State Resistance / R _{ON}		500	1000	mΩ
Off State Input to Output Isolation / R _{OFF}	TBD	10		GΩ
Channel to Channel Isolation	TBD	10		GΩ
Off / Open State Switch Rated Voltage (Input to Output) ⁴			+/- 150	V _{DC}
On / Closed State Switch Rated Voltage (Input to Output)			+/- 45	V _{DC}
Switching Time		8	10	μsec
Full Cycle Frequency			10	kHz
Mechanical Reliability	3x10 ⁹			Cycles
Electrical Reliability (1.0V, 10mA)	3x10 ⁹			Cycles
Leakage Current @ 150 Volts		< 19		pA

³ Duty Cycle based on 10 us period. Average current over period and all channels must NOT exceed *Total Current per Device* specification.

⁴ The voltage difference between RF Output (Beam) pin and Supply Voltage Return (VSS) pin must be ±2.5V.

Table 2 Recommended Operating Conditions, DC and AC Electrical Characteristics
(continued)

Parameter	Minimum	Typical	Maximum	Unit
High Voltage Gate Bias (VBB)	67.5	70	72.5	V _{DC}
High Voltage Gate Bias (VBB) Supply Current			0.1	mA
Low Voltage Supply (VDD)	4.5	5.0	5.5	V _{DC}
Low Voltage Supply (VDD) Current (standby)			50	uA
SPI Clock Frequency (CLK)	0.5		5	MHz
SPI Logic Level (High)	3.5	5.0	5.3	V
SPI Logic Level (Low)	-0.3	0.0	0.8	V
SPI Pulse Duration, clock high	100			nS
SPI Pulse Duration, latch enable high	100			nS
SPI Setup Time, data before clock	50			nS
SPI Hold Time, data after clock	50			nS
SPI Delay Time, clock to latch enable high	50			nS
SPI Propagation Delay Time, latch enable to output		300		nS
Operating Temperature Range	-40		+85 (MM1200-00) +100 (MM1200-00-E)	°C

Typical Performance Characteristics

Note: All measurements performed on MM1200-EVK test and evaluation board

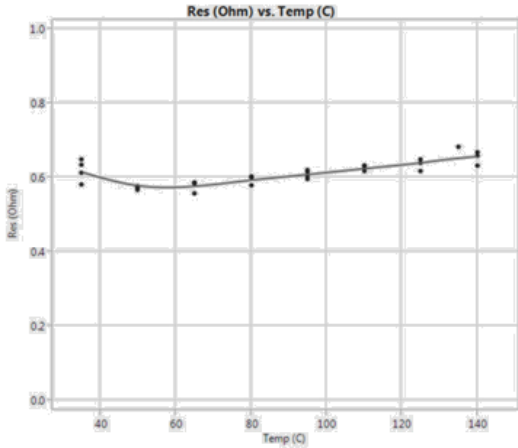


Figure 7 Resistance vs Temperature

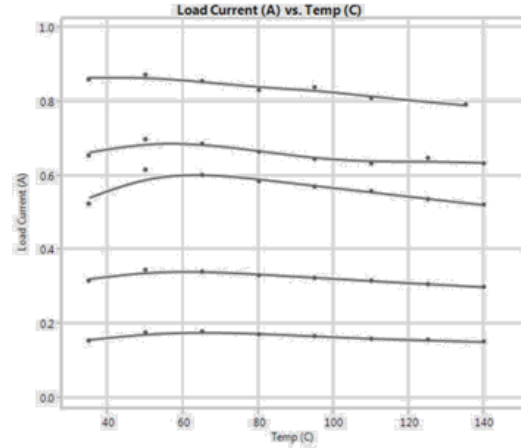


Figure 8 Load Current vs Temperature

49-Lead BGA Package Pin Out

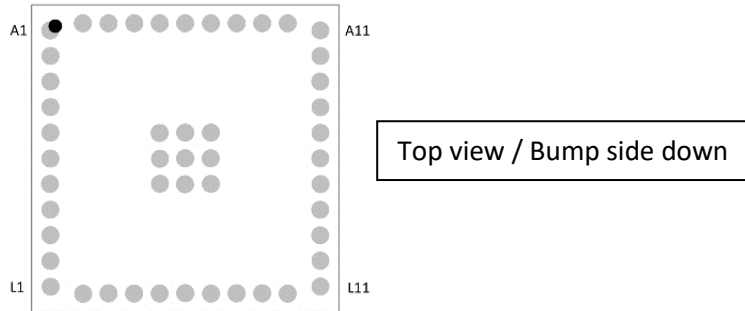


Table 3 Detailed Pin Description

Pin #	Function	Description	Pin #	Function	Description
A1, C1, J1, L1, L2, L4, L6, L8, L10, L11, J11, C11, A10, A11, A6, A8, A2, A4, E5, E6, E7, F5, F6, F7, G5, G6, G7	GND	Ground Reference	L9	IN5	Input (Contact 5)
B1	OUT1	Output (Beam 1)	K11	IN6	Input (Contact 6)
D1	BLNK	All Channels Off	H11	CLK	SPI Clock Input
E1	SDI	SPI Serial Data Input	G11	VSS	Supply Voltage Return
F1, D11	N/C	Do Not Connect	F11	VDD	+5 VDC Logic Supply
G1	VBB	High Voltage Supply	E11	LE	SPI Strobe Input
H1	SDO	SPI Serial Data Output	B11	OUT6	Output (Beam 6)
K1	IN1	Input (Contact 1)	A9	OUT5	Output (Beam 5)
L3	IN2	Input (Contact 2)	A7	OUT4	Output (Beam 4)
L5	IN3	Input (Contact 3)	A5	OUT3	Output (Beam 3)
L7	IN4	Input (Contact 4)	A3	OUT2	Output (Beam 2)

SPI Interface Gate Drive Control

Operating Description

The SPI bus gate driver block diagram is shown in Figure 22 below. The driver contains a 10-bit shift register and 10-bit latch. This interface uses only registers and latches 6-1. Registers 10-7 are not connected. The high voltage driver is controlled by the Clock, Data In, Latch Enable, and Blanking lines as follows:

- A 6-bit data word is serially loaded into the shift register on the positive-going transition of the clock. First bit loaded ends up in register 6, last bit in register 1.
- Parallel data is transferred to the output buffers through a 10-bit D latch while the latch enable input is pulsed high. Only latches 6-1 are connected internally.
- Data is latched when the Latch Enable is low.
- If Latch Enable remains high, the latches operate in transparent mode.
- When the Blanking is high; all of the outputs are low.
- All inputs are compatible with 5V CMOS levels.
- Serial Data Out is available for cascading devices (extra clocks needed to pass data through registers 7-10)

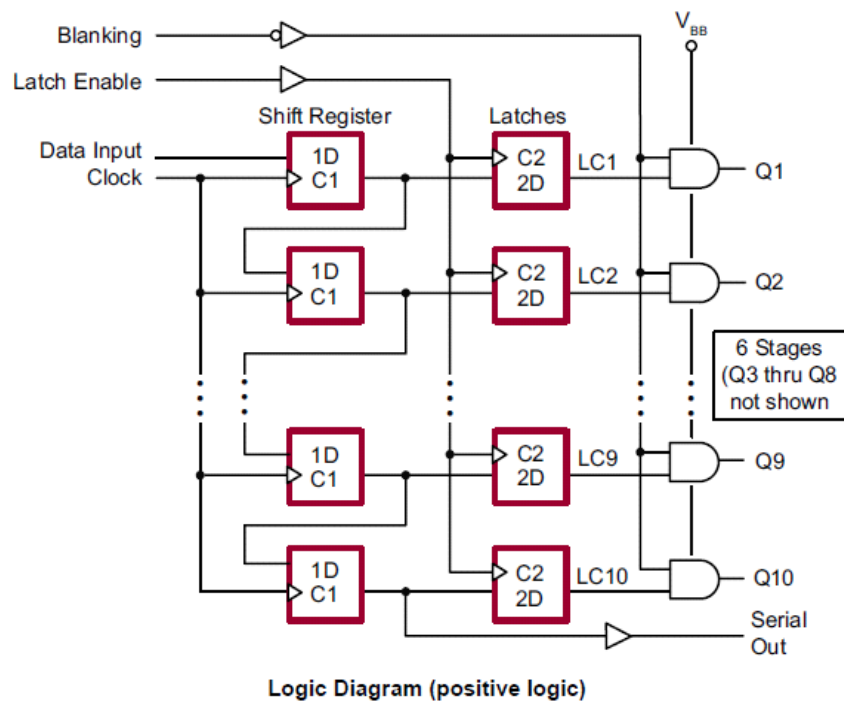


Figure 10 High Voltage Gate Driver Block Diagram

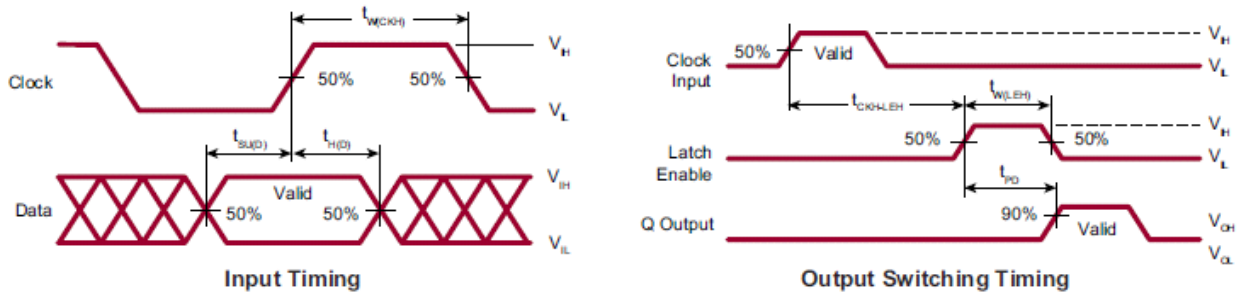
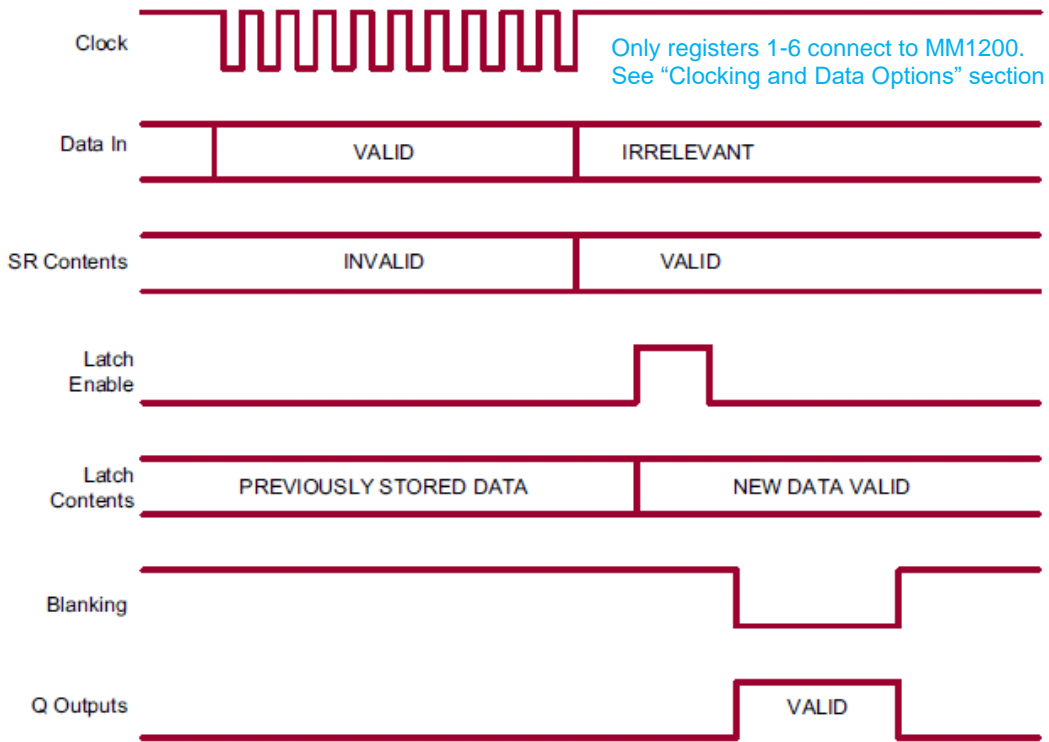





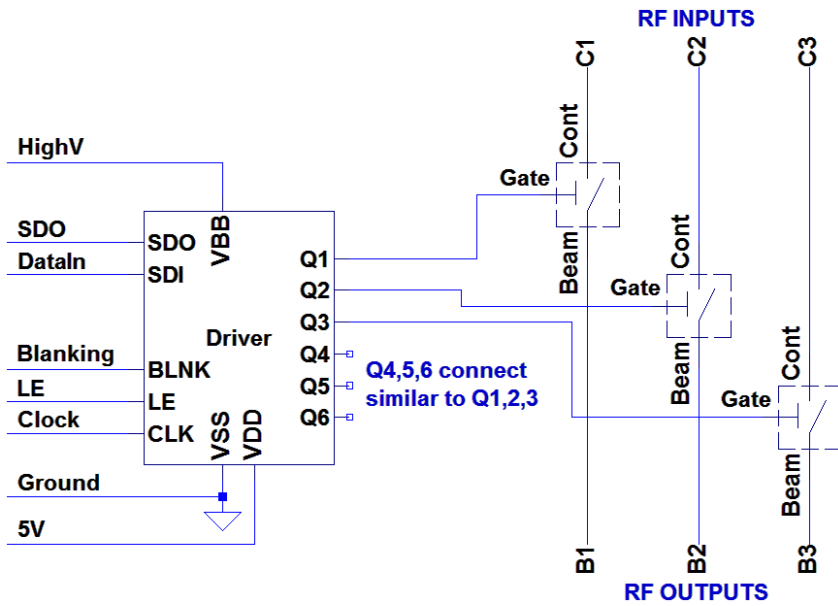

Figure 11 Switching Waveforms

Figure 12 Timing Diagram

Table 4 Digital Control Functions

Serial Data Input	Clock Input	Shift Register Contents $I_1 I_2 I_3 \dots I_{N-1} I_N$	Serial Data Output	LE Strobe Input	Latch Contents $I_1 I_2 I_3 \dots I_{N-1} I_N$	Blanking Input	Output Contents $I_1 I_2 I_3 \dots I_{N-1} I_N$
H		$H R_1 R_2 \dots R_{N-2} R_{N-1}$	R_{N-1}	---	---	---	---
L		$L R_1 R_2 \dots R_{N-2} R_{N-1}$	R_{N-1}				
X		$R_1 R_2 R_3 \dots R_{N-1} R_N$	R_N				
---	---	$X X X \dots X X$	X	L	$R_1 R_2 R_3 \dots R_{N-1} R_N$	L	$P_1 P_2 P_3 \dots P_{N-1} P_N$
		$P_1 P_2 P_3 \dots P_{N-1} P_N$	P_N	H	$P_1 P_2 P_3 \dots P_{N-1} P_N$		
		---	---	---	$X X X \dots X X$		

Notes:
L = Low logic level, H = High logic level, X = Don't care, P = Present state, R = Previous state
 = Low to high transition

 = High to low transition

Figure 13 Simplified Functional Block Diagram

Clocking and Data Options

The driver section has a 10-bit shift register and latch. However, only registers 1-6 are connected to the 6 MM1200 channels in this device. Registers 7 to 10 are unused, except that data must be shifted through them if you wish to cascade devices. The MM1200 provides a Serial Data Output (SDO) pin, which enables cascading this device for additional switch channel applications. Other devices can be daisy-chained by connecting the SDO of one device to SDI of another.

Test and Evaluation Board

Technical Description

A test and evaluation board kit MM1200-EVK is available as shown in Figure 14 below to verify the performance of the MM1200, and is flexible enough to incorporate into various R&D experimental designs. The signal layer is 0.020" thick Rogers Corporation 4350B material, $\epsilon_r = 2.94$. The metal layers are 1.0 ounce copper with gold plated top and bottom layers with end launch stainless steel SMA female connectors.

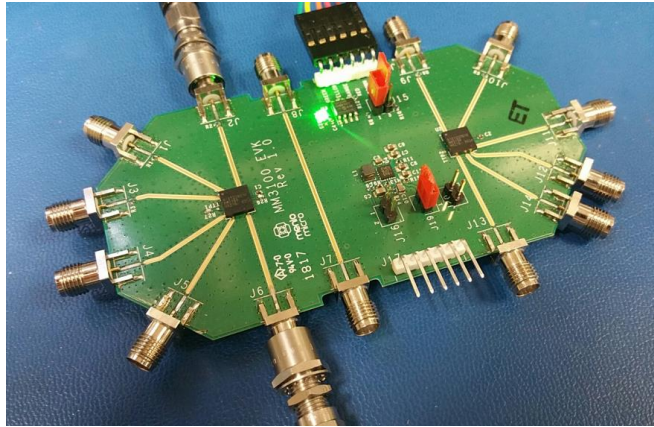


Figure 14 MM1200-EVK Test and Evaluation Board

Evaluation Board USB Interface Cable

The USB interface cable pictured in Figure 15 below is used for connecting up the MM1200 test and evaluation board. This cable provides the required +77.5 volt bias and digital SDI bus data for controlling the 6 SPST switches.



Figure 15 MM1200-EVK USB Interface Cable

Recommended PCB Layout and SMT Parameters

- PCB lands should be as shown in the pad pattern diagram.
- Open space around the package can have grounded thru holes.
- Use ENIG pad surface finish.
- Use 100 micron thick Soldermask.
- Use Type 3 or higher Solder Paste with no clean Flux.
- Component placement force should not exceed 100 grams.

Recommended PCB Pad Pattern

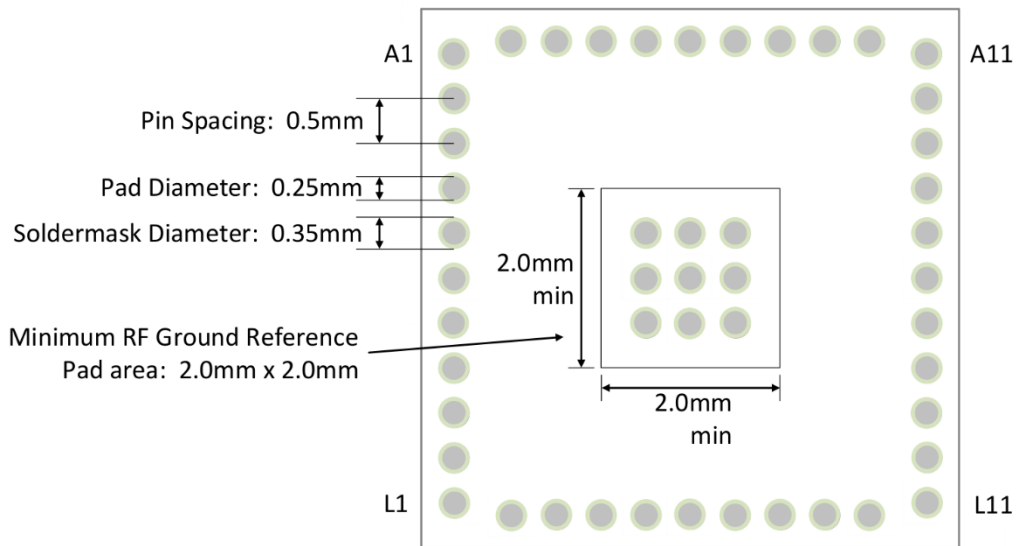
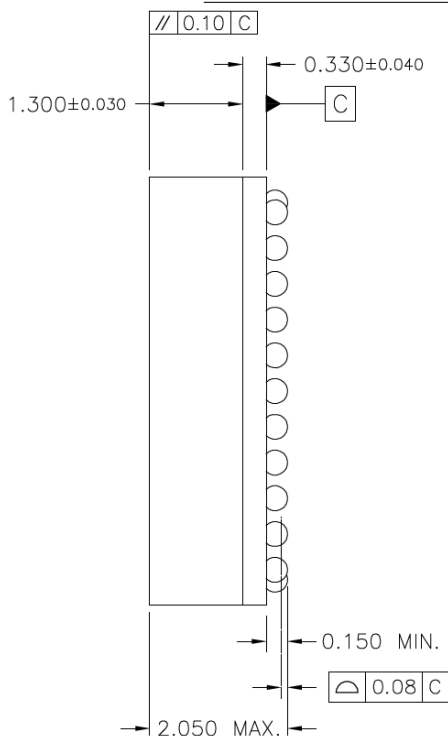
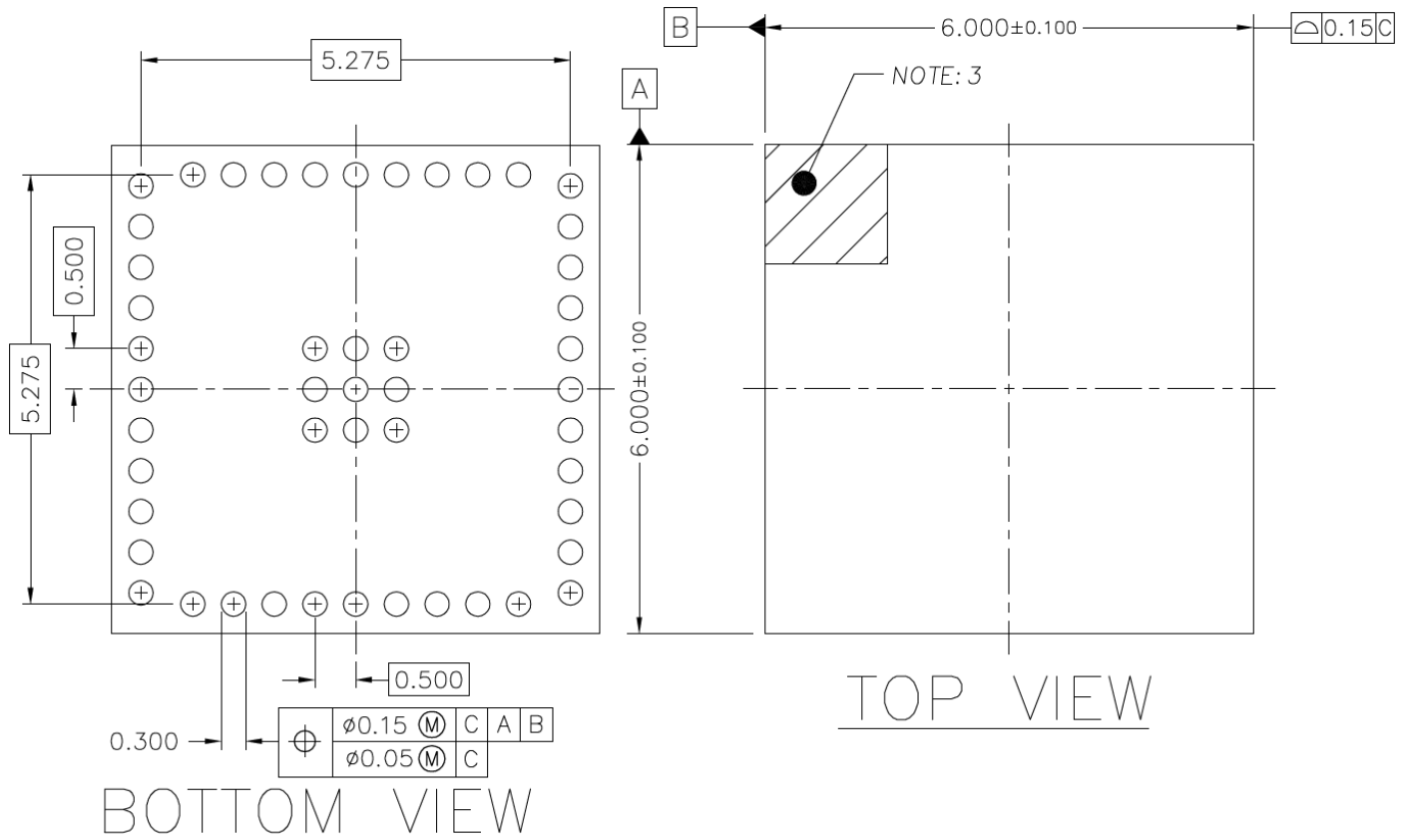


Figure 32 Recommended PCB Pad Pattern

Package Dimensions – 49 Lead Ball Grid Array
0.30mm Ball, 0.50mm Pitch

NOTES :

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSIONS ARE IN MM.
3. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
4. SOLDER BALLS, ARE LEAD FREE SOLDER.
5. REFER TO JEDEC PUBLICATION 95 DESIGN GUIDE 4.5 FINE-PITCH SQUARE BALL GRID ARRAY PACKAGE FOR DATUMS. FEATURES AND DIMENSIONS NOT SHOWN.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Package Marking Information

The MM1200 package marking and nomenclature is illustrated in Figure 33 below.

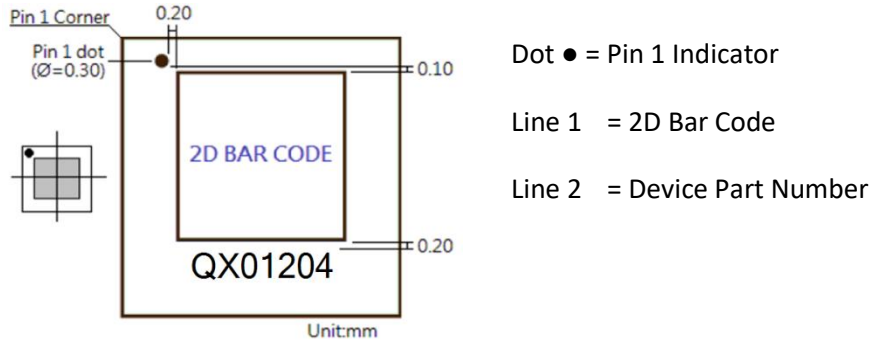


Figure 33 Package Markings

Ordering Information

Part Number	Package	Packaging
MM1200-00	6mm x 6mm x 1.3mm BGA	Tape and Reel
MM1200-00-E	6mm x 6mm x 1.3mm BGA	Tape and Reel

Important Information

Disclaimer

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