Through Glass Via (TGV) Technology for RF Applications

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Abstract

Over the past several years there have been substantial advancements in through glass via (TGV) technology. There is an excellent opportunity to leverage TGV technology and the insulating properties of glass, to address next generation needs for RF components. Multi-bands multi-standards with carrier aggregation, WiFi/GPS coexistence, and LTE-U make RF front end more and more complicated. In order to address the best-fit filtering solutions to RF front end, high-performance inductors and capacitors are required. For inductors, drastic performance (size and Q) improvement have been demonstrated by technology evolutions from 2D planar inductors on glass to 3D solenoid using TGV, achieving inductor Q>80 (for 3nH @ 1GHz). On top of the TGV inductors , we have successfully integrated Cu MIM (metal-insulator-metal) capacitors by using 15um thick Cu plates, resulting in Q>560 (10pF @ 2GHz).

Key words

Glass, Through Glass Via (TGV), RF components, High-Q 3D inductor, High-Q Cu MIM

I. Introduction

In RF front end (anywhere between antenna and amplifiers), there are many passive circuits required to provide the best filtering solutions for the multi-band multi-standards. The filtering solution at the RF front end requires the lowest insertion loss with wide frequency range bands-grouping LC filters, combined with specific band selecting narrow band acoustic filters. Fig. 1 shows example filter topologies for low-pass filters composed of multiple inductors (L) and capacitors (C), depending on insertion loss and rejection requirements. The low pass filters have been used for power amplifier (PA) module, filtering out harmonics from the PA. More recently, with the commercialization of carrier aggregation, diplexer (low pass + high pass filters), triplexer (low pass + mid band pass + high pass filters), and multiplexers are becoming more important. The multiplexers are filtering groups of bands (B1, B2, …, B40) using multiple lumped elements (L and C). This work will mainly focus on the recent achievements in design and technology demonstration for both high-Q L and C components co-fabricated in a TGV platform.

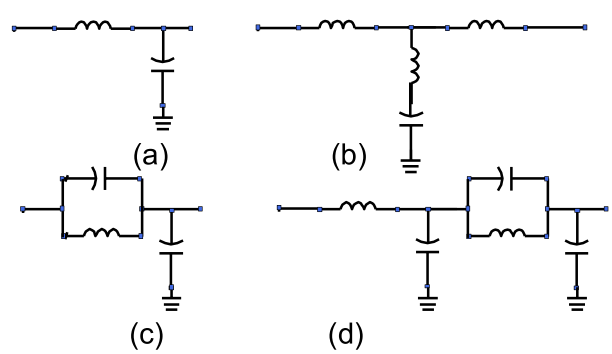
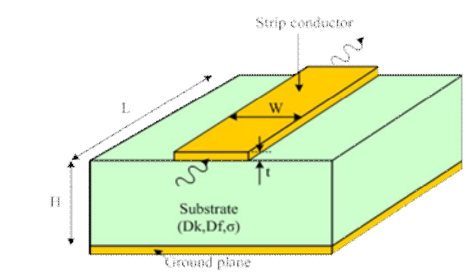


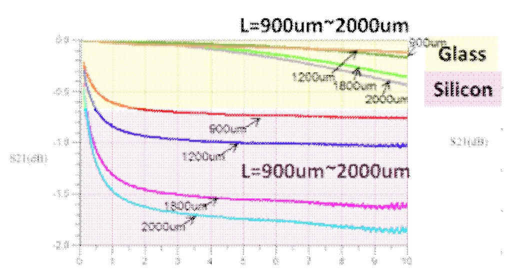
Fig.1 LC-based low-pass filters composed of (a) 1L+1C, (b) 3L+1C, (c) 1L+2C, (d) 2L+3C components.

Glass has many properties that make it an ideal substrate for RF components such as: ultra-high resistivity and low electrical loss providing opportunities for designers to use glass in new ways for advanced packaging applications [1]-[4]. As an illustration, Fig. 2 below shows an example of the insulating properties of glass that make it valuable in RF applications, particularly at high frequencies. Fig. 2 (a) shows the microstrip lines included in a test die to evaluate insertion loss of glass and silicon. The plot in Fig. 2(b) shows the results (each curve represents the insertion loss for lines 0.9, 1.2, 1.8 and 2.1 mm long). The tan region shows results from glass substrates and pink region highlights loss from silicon substrates at frequencies up to 10 GHz. The loss is significantly lower in glass substrates than it is in silicon substrates. This low loss given by the insulating properties of glass offers the important ability to achieve high Q-factors in filter applications.

The advantages given by Corning's fusion forming process for supplying substrates for electronics applications, has been previously reported [5], [6]. The fusion forming process, allows forming high quality substrates in large formats 0.5 meter or larger, which results in cost reduction by leveraging economies of scale. Furthermore, the glass can be formed in thickness as low at 0.1 mm. The requirements for low loss, small package size and low cost make glass an ideal solution as RF components become increasingly pervasive in mobile devices.



(a)



(b)

Fig. 2 (a) Microstrip line structure, (b) Insertion loss for glass and silicon interposers. Insulation properties of glass have significant advantages in reducing insertion loss

II. TGV Passives Process

A. TGV glass process

Over the past several years, there have been significant advances in the ability to provide high quality vias in glass substrates of various formats at Corning, Incorporated. The process employed provides the opportunity to leverage both through and blind vias in both wafer and panel format. The glass substrates with holes have been shown to give strength on par with bare glass, and filled vias have been shown to have excellent mechanical and electrical reliability after thermal cycle tests [5]-[7]. The approximate current best practice capabilities are summarized in Table 1 below. These represent guidance for the current TGV process, but in many cases some capabilities can be extended.

Table 1 State-of-the-art TGV specification

Attribute	Current Capability*
Outer Diameter (OD)	25 – 100 um
Minimum Pitch	~2x OD
Type	Through and Blind
Wafer Size	Up to 300 mm
Panel Size	Up to 515 x 515 mm
Thickness (mm)	0.1 – 0.7

*Approximate – Some specifications can be negotiated

The work described here utilized glass with thickness of ~0.4 mm thick and through glass via (TGV) diameter of 80 um. A profile of a typical TGV profile is shown in Fig. 3.

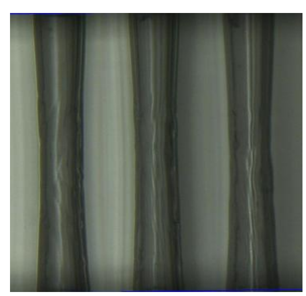


Fig. 3 Image of 80 um diameter TGV in 0.4 mm thick glass.

B. TGV IPD (integrated passive devices) integration

The process flow of TGV and IPD integration is shown in Fig. 4. First of all, TGVs of 80µm in diameter and 150-200µm in pitch were formed on a 400µm thick alkali-free glass wafer. 50nm Ti and 1000nm Cu layers were deposited as Cu seed materials. Then the TGV sidewall and front side and backside metal layers were formed with 15µm Cu thickness by conformal electroplating. By this time, functional 3D TGV inductors were formed. Also, parts of front side Cu serve as a capacitor bottom plate.

Silicon Nitride film was deposited on the front side metal as capacitor dielectric using PECVD. After 2µm thick Cu layer formed on Silicon Nitride as a capacitor top electrode, the Silicon Nitride film outside the capacitor area was etched by RIE to create an MIM capacitor.

Thick dielectric polymer layer was laminated on the wafer as RDL passivation film using photosensitive polyimide followed by low temperature cure of 210 degree Celsius. Redistribution lines were patterned with positive photo resist. Cu RDL line of 15 µm thickness was deposited by Cu-electroplating followed by photo resist and Cu seed layer removal.

The TGV IPD wafers were then ball-attached on the solder mask openings and diced individually using laser dicing methods.

III. Results

Fig. 5 shows 3D rendering of inductor structure, inductor top-down view, and cross-sectional SEM of a fabricated 3D inductor. The SEM (scanning electron microscope) image shows uniform conformal plating with 15µm thick Cu. The conformal plating method has great advantage of process time of plating. The key requirement for conformal plating method is coverage of seed metal layer in the vias. The sputtering angle was optimized for the 400 µm deep TGV metallization. Conformal Cu metallization of TGV in a 200 mm wafer level was successfully achieved by electroplating.

The simulated inductance and Q are 3.0nH and 83 at 1GHz, respectively, for the inductor in Fig. 5. The peak Q was observed to be 200 at 4GHz. This is one of the highest inductor Q reported.

Fig. 6 shows the MIM capacitor formed on the same TGV glass substrate. With the 15um bottom Cu plate and 17um top Cu plate, also record high-Q MIM capacitor was achieved: Q=560 at 2GHz for 10pF capacitor.

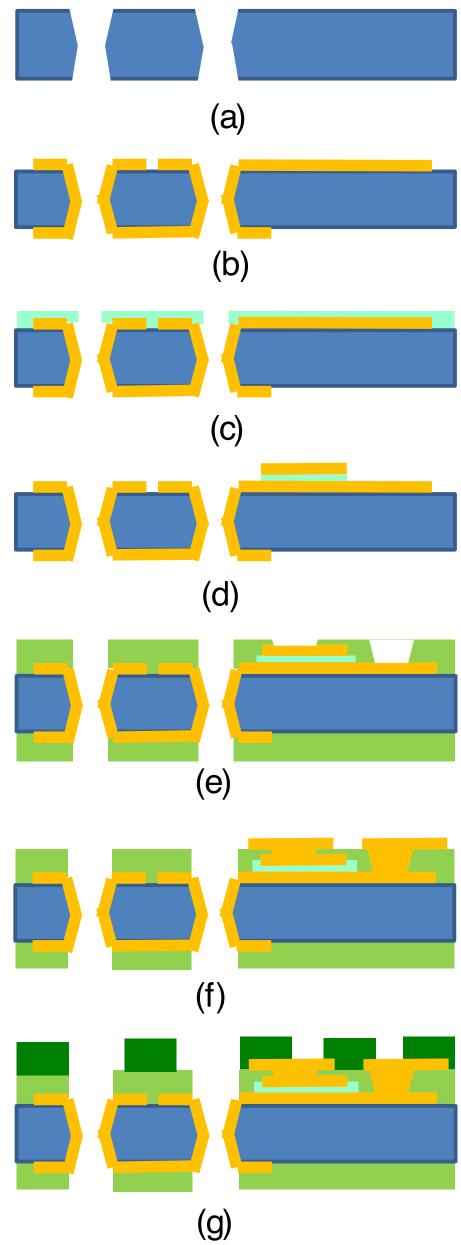


Fig. 4 TGV IPD inductor-first, MIM-last process flow. (a) Starting TGV glass wafer, (b) inductor formation by patterning and plating front side, backside, and TGV sidewall simultaneously. (c) MIM dielectric formation by silicon nitride deposition. (d) MIM top plate by Cu plating then silicon nitride etching outside MIM area, (e) front side and backside interlayer

dielectric pattern, (f) final Cu interconnects and pads, (g) solder resist formation around the I/O pads.

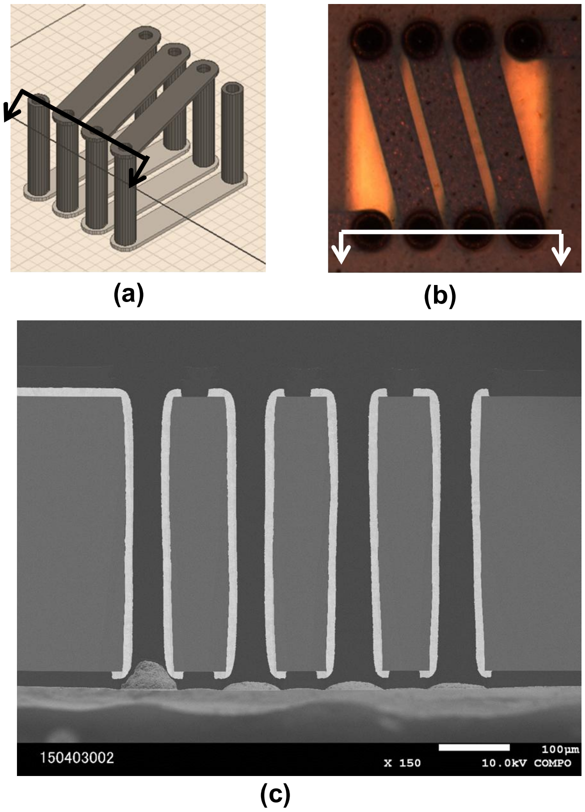


Fig. 5 3D TGV inductor formation. (a) 3D rendering, (b) top-down photograph, (c) cross-sectional SEM of TGV with conformal Cu plating on the TGV sidewalls and the top & bottom sides of the glass to form a 3D TGV inductor

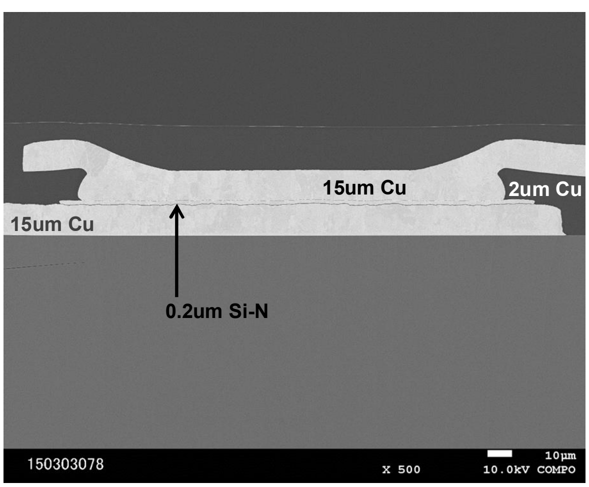


Fig. 6 Cross-sectional SEM of TGV with conformal Cu plating on the TGV sidewalls and the top & bottom sides of the glass to form a 3D TGV inductor

Fig. 7 shows a complete die of RF multi-band filters in a single chip with WLCSP solder balls attached and completely singulated using laser dicing.

The TGV IPD parts were mounted on evaluation boards and further tested for both electrical functionality and thermal and mechanical reliability, showing no performance degradation or any board-level reliability issues.

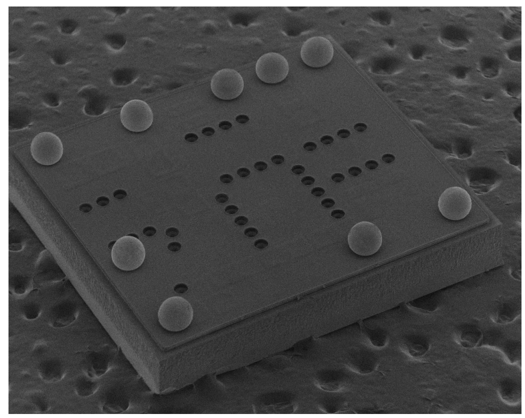


Fig. 7 SEM bird's eye view of completed LC networks for RF front end filters.

IV. Conclusion

Glass has a number of attributes that make it an excellent substrate for RF applications. Since glass is an insulating material, its electrical properties provide a low loss substrate for high-Q inductors. The ability to generate well-formed through vias has been demonstrated, and has been shown to be reliable in electrical and thermal testing. Furthermore, manufacturing processes to form glass in thin large sheets of high quality is mature and gives opportunity to reduce cost through economies of scale. These characteristics generate tremendous incentive for using glass as a TGV substrate for RF applications. Using the TGV technology, high-performance integrated LC networks were co-fabricated with unprecedented electrical performance and reliable process integrity.

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